

WHAT IS CLAIMED IS:

1        1. A circuit for controlling two switches bidirectional for the voltage and  
2 unidirectional for the current, assembled in anti-parallel, comprising, in series  
3 between two terminals of the anti-parallel assembly, two identical control stages  
4 respectively dedicated to each switch and between which is interposed a common  
5 impedance setting a phase angle for the turning-on of the switches, each stage  
6 comprising:

7            a controllable current source for providing a current to a control electrode of  
8 the concerned switch;

9            a capacitor for storing a supply voltage of at least the current source;

10            an element of activation/deactivation of the current source according to the  
11 voltage across the stage capacitor; and

12            an assembly for discharging the capacitor during the operation of the other  
13 stage.

1        2. The circuit of claim 1, wherein said current source is sized to control  
2 the di/dt at the switching-on of the concerned switch.

1        3. The circuit of claim 1, wherein said discharge assembly is activated as  
2 soon as the current in the concerned switch is canceled.

1        4. The circuit of claim 1, wherein the capacitor of each stage is in series  
2 with a first diode, between the impedance and the stage terminal which is the same  
3 as the terminal of the anti-parallel assembly.

1        5. The circuit of claim 4, wherein a second diode of each stage connects  
2 said impedance with said terminal of the stage which is the same as the anti-parallel  
3 assembly terminal.

1        6. The circuit of claim 5, wherein a third diode connects the control  
2 electrode of the switch of each stage to the electrode of said capacitor, so that said  
3 discharge assembly also discharges the control electrode of the stage switch.

1        7. The circuit of claim 1, wherein the respective capacitor of each stage  
2 provides the power supply necessary to all stage components.

1           8. The circuit of claim 1, wherein said activation/deactivation element  
2 activates said current source with which it is associated when the voltage across the  
3 capacitor of the stage becomes greater than a first threshold, itself greater than the  
4 threshold voltage of the concerned switch.

1           9. The circuit of claim 8, wherein said comparator deactivates said current  
2 source with which it is associated when the voltage across the capacitor of the stage  
3 becomes greater than a second threshold, itself preferably smaller than said  
4 threshold voltage of the concerned switch.

1           10. The circuit of claim 1, wherein each discharge assembly comprises a  
2 first transistor in parallel with the stage capacitor, the control electrode of the first  
3 transistor being connected, via a second transistor, to said impedance.

1           11. The circuit of claim 1, wherein said activation/deactivation element of  
2 each stage is formed of a comparator receiving at a first input the voltage across the  
3 stage capacitor and at a second input a reference voltage, said comparator being  
4 supplied by the voltage across the capacitor of the concerned stage.

1           12. The circuit of claim 1, wherein said impedance is formed of a  
2 potentiometer.

1           13. The circuit of claim 1, wherein said impedance is formed of a first  
2 resistor in parallel with a second switchable resistor, said first resistor having a much  
3 greater value than the second one.

1           14. A power dimmer of a load, comprising the circuit of claim 1.

1           15. A circuit for controlling a motor, comprising the circuit of claim 1.

1           16. A power-reducing circuit, comprising:

2           a load node;

3           a supply node operable to receive a time-varying supply signal having a  
4 positive half period during which the load node is positive relative to the supply node  
5 and having a negative half period during which the load node is negative relative to  
6 the supply node;

7           a first switch coupled to the load node and to the supply node;

8           a second switch coupled to the load node and the supply node;

9           a first control stage coupled to the load node and operable to close the first  
10   switch during a portion of the positive half period of the supply signal; and  
11           a second control stage serially coupled between the first control stage and the  
12   supply node and operable to close the second switch during a portion of the  
13   negative half period of the supply signal.

1           17. The power-reducing circuit of claim 16 wherein the time-varying signal  
2   comprises a sinusoidal voltage signal.

1           18. The power-reducing circuit of claim 16 wherein:  
2           the first control stage is operable to open the first switch when a current  
3   through the first switch decays to approximately zero; and  
4           the second control stage is operable to open the second switch when a  
5   current through the second switch decays to approximately zero.

1           19. The power-reducing circuit of claim 16 wherein the first control stage  
2   comprises:

3           a capacitor operable to receive a charging current during the positive half  
4   period of the supply signal;  
5           a comparator operable to close the first switch when a voltage across the  
6   capacitor exceeds a first reference voltage and to open the first switch when the  
7   voltage across the capacitor is less than a second reference voltage; and  
8           a discharge circuit operable to discharge the capacitor when the charging  
9   current decays to approximately zero.

1           20. The power-reducing circuit of claim 16 wherein the second control  
2   stage comprises:

3           a capacitor operable to receive a charging current during the negative half  
4   period of the supply signal;  
5           a comparator operable to close the second switch when a voltage across the  
6   capacitor exceeds a first reference voltage and to open the second switch when the  
7   voltage across the capacitor is less than a second reference voltage; and  
8           a discharge circuit operable to discharge the capacitor when the charging  
9   current decays to approximately zero.

1           21. The power-reducing circuit of claim 16, further comprising an  
2 adjustable impedance serially coupled between the first and second control stages.

1           22. A system, comprising:

2           first and second supply nodes operable to receive a time-varying supply  
3 signal having a positive half period during which the first supply node is positive  
4 relative to the second supply node and having a negative half period during which  
5 the first supply node is negative relative to the second supply node;

6           a load having a first node coupled to the first supply node and having a  
7 second node; and

8           a power-reducing circuit coupled between the second node of the load and  
9 the second supply node and comprising,

10           a first switch coupled between the load and the second supply  
11 node,

12           a second switch coupled between the load and the second  
13 supply node,

14           a first control stage coupled to the load and operable to close the  
15 first switch during a portion of the positive half period of the supply signal; and

16           a second control stage serially coupled between the first control  
17 stage and the second supply node and operable to close the second switch  
18 during a portion of the negative half period of the supply signal.

1           23. The system of claim 22 wherein the load comprises an inductive load.

1           24. A method, comprising:

2           driving a load with a time-varying signal;

3           charging a first capacitor with a first current that flows through the load during  
4 a first portion of the signal;

5           causing a second current to flow through the load when a voltage across the  
6 first capacitor exceeds a first predetermined voltage; and

7           prohibiting the second current from flowing through the load when the voltage  
8 across the first capacitor decays to approximately a second predetermined voltage.

1           25. The method of claim 24, further comprising adjusting a time that the  
2 second current flows through the load by adjusting the first current.

1           26. The method of claim 24 wherein a total current through the load equals  
2 a sum of the first and second currents.

1           27. The method of claim 24 wherein the second current is significantly  
2 greater than the first current.

1           28. The method of claim 24 wherein:  
2           causing the second current to flow comprises closing a switch in series with  
3 the load; and  
4           prohibiting the second current from flowing comprises opening the switch.

1           29. The method of claim 24 wherein:  
2           causing the second current to flow comprises activating a transistor in series  
3 with the load;  
4           prohibiting the second current from flowing comprises deactivating the  
5 transistor; and  
6           the second predetermined voltage comprises a threshold of the transistor.

1           30. The method of claim 24, further comprising:  
2           charging a second capacitor with a third current that flows through the load  
3 during a second portion of the signal;  
4           causing a fourth current to flow through the load when a voltage across the  
5 second capacitor exceeds a third predetermined voltage; and  
6           prohibiting the fourth current from flowing through the load when the voltage  
7 across the second capacitor decays to approximately a fourth predetermined  
8 voltage.

1           31. A method, comprising:  
2           driving a load with a time-varying signal;  
3           charging a capacitor with a first current that flows through a load during a first  
4 portion of the signal;  
5           causing a second current to flow through the load when a voltage across the  
6 capacitor exceeds a predetermined voltage; and  
7           prohibiting the second current from flowing through the load when the first  
8 current decays to approximately a predetermined current.

1           32. The method of claim 31 wherein the predetermined current equals zero  
2 current.